51. The ATM switch according to claim 42, wherein the rate limitation is enforced at inputs.

52. The ATM switch according to claim 42, wherein the rate limitation is enforced at outputs.

53. The ATM switch according to claim 42, wherein each of the data units designates a priority and an input port and the determination of whether the additional data units which designate relatively low priorities and a particular input port are in violation of the rate limitation is based on a "leaky bucket" algorithm.

54. The ATM switch according to claim 53, wherein the particular input port is associated with a selected store whose backlog caused the selective filtering condition to be imposed.

**REMARKS**

Claims 1-5, 7-16 and 18-54 are currently pending in this application. Claims 1, 7, 10, 11, 12, 18 and 23 have been amended and claims 6 and 17 have been cancelled. Applicant respectfully submits that the claims currently pending in this case are patentably distinguishable over the cited references, and reconsideration and allowance are respectfully requested

In an Office Action date August 10, 2001, the Examiner objected to the drawings under 37 C.F.R 1.83(a) for allegedly failing to show output controls arranged to monitor the backlog of data units buffered in two or more of the plurality of data stores for delivery to their associated output ports. Applicant has submitted herewith an amended FIG. 3 such that data buffer 340 comprises a plurality of operatively distinct data stores e.g. (Data $Store_1$ through Data $Store_P$). The proposed changes are shown in redline in the amended drawing. The proposed changes are supported by the originally filed specification

which teaches that data buffer 340 in FIG. 3 "has operatively distinct stores for buffering data units according to their particular characteristic, such as priority. For a switch supporting P levels of priority, data buffer 340 preferably has P stores for separately buffering data units for each particular priority". (page 8, lines 2-3). Applicant therefore respectfully submits that no new matter has been added and requests that the amended drawing be entered and the objection withdrawn.

The Examiner objected to claim 23. Applicant has amended claim 23 in accordance with the Examiner's suggest to correct the objected to informality and therefore respectfully requests that this objection be withdrawn.

The Examiner rejected claims 33-54 under 35 U.S.C. 112 first paragraph for allegedly failing to provide support for the limitation of "output controls are arranged to monitor the backlog of buffered data units in two or more of the plurality of data stores for delivery to their associated output ports."

With reference to FIGS. 3 and 7, the originally filed specification teaches that "Each time a data unit is buffered in one of the P stores within data buffer 340, output control 350 increments a backlog value in memory corresponding to the store so that the current backlog of data units stored in each store is determinable by output control 350 by reference to the incremented value." (page 8, lines 13-16). The originally filed specification further teaches that "output control 350 monitors the P backlog values (700) and compares any one, any desired combination or all of the backlog values with selected maximum values to determine if a maximum has been exceeded (710)." (page 10, lines 8-10). Applicant therefore submits that the originally filed specification clearly teaches an output control arranged to monitor the backlog of buffered data units in two or more data store. Accordingly, Applicant respectfully requests that this rejection be withdrawn.

The Examiner rejected claims 1, 5-10, 16-20, and 22 under 35 U.S.C. 102(e) as allegedly being anticipated by Ramamurthy et al (U.S. Pat. No. 6,046,901). Applicant respectfully traverses this rejection.

Independent claims 1 and 10 recite an ATM switch wherein each of a plurality of output ports are "operatively associated with a plurality of output data stores and an output control." The cited reference does not disclose or suggest a switch having a plurality of output ports, wherein each of the output ports is operatively associated with a plurality of output data stores. Rather, referring to FIG. 9 and col. 22 lines 42-52, Ramamurthy discloses an ATM switch having two input ports (910, 920) with traffic streams directed to certain output port(s). Each output port is operatively associated with only a single 128 cell output buffer that serves the two input ports in a work-conserving, round-robin manner.

Therefore, applicant respectfully submits that claims 1 and 10 each recite a novel and unobvious apparatus in view of Ramamurthy and should therefore be allowed. Further claims 2-5, 7, and 9 and claims 11-16, 18 and 20-22, that depend on claims 1 and 10 respectively are allowable as are claims 1 and 10 and for the additional limitations recited therein.

The Examiner rejected claims 23, 28-30, and 32 under 35 U.S.C. 103(a) as allegedly being obvious over Ramamurthy in view of Khacherian et al. (U.S. Patent 5,768,257). This rejection is respectfully traversed. It is respectfully submitted that Khacherian cannot properly be used as a § 102(e) reference in a § 103(a) rejection. 35 U.S.C. 103(c) states that "Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f) and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and claimed invention were, at the time of the invention was made, owned by the same person or subject to an obligation of assignment to the same person."

The claims presently pending are entitled to a priority date of January 14, 1998 in accordance with the filing date of the parent application. Khacherian issued after the priority date of the claims pending in the current application and can therefore only prior art, if at all to the present pending claims under 35 U.S.C. 102(e). In addition, Khacherian and the present application are both assigned to a common assignee, namely Xylan Corporation, of Calabasas, CA. Therefore Khacherian can not be properly utilized as a section 102(e) reference in combination with a section 103 rejection of the claims presently pending in this application.

Accordingly, applicant respectfully submits that claim 23 is allowable over the cited references. Further claims 24-32, that depend on claim 23 are allowable as is claim 23 and for the additional limitations recited therein.

The Examiner rejected claims 33, 37-42, 48-52 and 54 under 35 U.S.C. 103(a) as allegedly being obvious over Ramamurthy in view of Shinohara (U.S. Patent 6,122,251). The Examiner admits that Ramamurthy does not specifically disclose an ATM switch having output controls that monitor two or more data stores. However, the Examiner alleges that Shinohara (see FIG. 8) teaches a flow control system wherein an output control monitors the backlog of two or more data stores. The Examiner therefore alleges that it would have been obvious to one of skill in the art to combine the rate control method taught by Shinohara with the switch of Ramamurthy. Applicant respectfully traverses this rejection.

Independent claims 33 and 42 recite an ATM switched comprised in part by "a plurality of output ports, each output port operatively associated with a plurality of data stores and an output control". Further as recited in independent claims 33 and 42 the output controls are "arranged to monitor the backlog of buffered data units in two or more of said plurality of data stores". Applicant respectfully

submits that cited references alone or in combination do not disclose or suggest the claimed elements.

Rather, referring to FIG. 8, Shinohara discloses a switch control circuit wherein a buffer occupancy measuring unit is used to measure the occupancy of a plurality of output buffers each of which is individually associated with a different output port. Shinohara simply allows a single output control to monitor the occupancy rate of each of the output ports rather than having an individual output control for each port. Shinohara does not however disclose or suggest an output control arranged to monitor the backlog of buffered data units in two or more output data stores, each of which is operatively associated with the same output port.

Accordingly, applicant respectfully submits that independent claims 33 and 42 recite a novel and unobvious apparatus in view of Ramamurthy and Shinohara and should therefore be allowed. Further claims 34-41 and claims 43-54, that depend on claim 33 and claim 42 respectively are allowable as are claims 33 and 42 and for the additional limitations recited therein.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By _____

Art Hasan
Reg. No. 41,057
626/795-9900

SAH/rlf

**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

In the specification:

A DIBOC-based ATM switch in accordance with the more preferred embodiment of the invention advantageously implements priority/port-based and a connection-based congestion control strategy. For that purpose, output control 580 must know the present backlog of data units buffered in the P stores in data buffer 550 corresponding to output port 540, and must know more generally backlog in the I x P stores in the aggregate of data buffers corresponding to output port 540. Output control 580 therefore has I x P physical memories. Each time a data unit is buffered in one of the P stores within data buffer 550 which corresponds to output port 540, output control 580 increments a backlog value in a memory corresponding to the store so that the current backlog of data units stored in each of the P stores is determinable by output control 580 by reference to the incremented values. More generally, each time a data unit is buffered in one of the I x P stores within one of the data buffers, output control 580 increments a backlog value in the corresponding memory. ~~Output~~ Input control 560 obtains buffering information through the transmission of "Requests". Thus, in the case of a flow from input port 510 to output port 540, input control 560 monitors data buffer 550 and for each buffered data unit destined for output port 540 transmits on line 515 a "Request" to release the data unit, which specifies the source input port and priority of the data unit. Output control 580 increments a value in the memory which corresponds to the specified source input port and priority.

In the claims:

1. (Amended) An ATM switch, comprising:

a plurality of input ports for receiving data units on virtual connections;

a plurality of output ports, each output port operatively associated with a plurality of output data stores and an output control; and

a switch fabric for switching data units from any of the input ports to any of the output ports;

wherein the output data stores are arranged to buffer data units for delivery to their associated output ports, and the output controls are arranged to monitor the backlog of buffered data units for delivery to their associated output ports and, if the backlog reaches a particular level, to enforce a rate limitation against additional data units for delivery to their associated output ports, wherein the additional data units in violation of the rate limitation are filtered.

7. (Amended) The ATM switch according to claim 1, wherein the data ~~buffers~~ stores are physically associated with output ports.

10. (Amended) An ATM switch, comprising:

a plurality of input ports for receiving data units on virtual connections;

a plurality of output ports, each output port operatively associated with a plurality of output data stores and an output control; and

a switch fabric for switching data units from any of the input ports to any of the output ports;

wherein the output data stores are arranged to buffer data units for delivery to their associated output ports, and the output controls are arranged to monitor the backlog of buffered data units for delivery to their associated output ports and, if the backlog buffered in one or more selected stores reaches a particular level, to a enforce a rate limitation against additional data units for delivery

to their associated output ports, wherein the additional data units in violation of the rate limitation are filtered.

11. (Amended) The ATM switch according to claim 10, wherein each output data store buffers data units having a distinct priority.

12. (Amended) The ATM switch according to claim 10, wherein each output data store buffers data units having a distinct priority and input port combination.

18. (Amended) The ATM switch according to claim 10, wherein the data ~~buffers~~ stores are physically associated with output ports.

23. (Amended) A DIBOC-based ATM switch, comprising:

a plurality of input ports for receiving data units on virtual connections, each input port physically associated with a plurality of data stores and an input control for transmitting "Requests" to release data units;

a plurality of output ports, each output port operatively associated with ~~a~~ the plurality of the data stores and physically associated with an output control for monitoring "Requests" to release data units; and

a switch fabric for switching data units for any of the input ports to any of the output ports;

wherein the data stores are arranged to buffer data units for delivery to their associated output ports, and the output controls are arranged to monitor the backlog of buffered data units for delivery to their associated output ports, through information transmitted in "Requests" and, if the backlog reaches a particular level, to enforce a rate limitation against additional data units for delivery to their associated output ports, wherein the additional data units in violation of the rate limitation are filtered.

JHG PAS395007.1-*-11/12/01 4:39 PM